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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,043	BYRNE ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-12,19 and 20* is/are rejected.

7)☒ Claim(s) *5-8 and 13-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-08-05

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 5-8,13-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4,9-12,19,20 are rejected under 35 U.S.C. 102(e) as being anticipated by Edwards et al. (US Publication Number 20030056154A1). As per claim 1, Edwards et al. discloses a plurality of processors on page 4, paragraph 0057, "It should be understood that any type of processor and any number of processors may be used."; a trace circuit configured to present information at a port for debugging software in a selected processor of said processors on page on page 5, paragraph 0072; a connector circuit configured to couple said trace circuit to said selected processor in response to a select signal and transfer said information from said selected processor to said trace circuit while said selected processor is executing said software on page 4, paragraph 0058 and page 5, paragraphs 0072-0073. The connector circuit is the communication

link 104 from the trace circuit to the selected processor. The trace circuit is part of the debug circuit as disclosed in Figures 2 and 3. Edwards et al. discloses a boundary scan chain connected to each of said processor and said trace circuit on page 11, paragraphs 0128,0129 and Figures 2 and 3.

4. As per claim 2, Edwards et al. discloses wherein said connector circuit is further configured to transfer data from said trace circuit to said selected processor on page 4, paragraph 0058 and page 5, paragraphs 0072-0073.

5. As per claim 3, Edwards et al. discloses wherein said connector circuit is further configured to transfer a first test data stream received by said selected processor through said boundary scan chain to said trace circuit on page 4, paragraph 0058 and page 5, paragraphs 0072-0073; on page 11, paragraphs 0128,0129 and Figures 2 and 3.

6. As per claim 4, Edwards et al. discloses wherein said connector circuit is further configured to transfer a second test data stream from said trace circuit through said boundary scan chain to said selected processor on page 4, paragraph 0058 and page 5, paragraphs 0072-0073; on page 11, paragraphs 0128,0129 and Figures 2 and 3.

7. As per claim 5, Edwards et al. discloses a first circuit configured to transfer said information from said selected processor to said trace circuit, transfer data from said trace circuit to said selected processor, and present a predetermined logic state to said processors other than said selected processor; and a second circuit configured to transfer a first test data stream received by said selected processor to said trace circuit, transfer a second test data stream from said trace circuit to said selected processor,

and present a second predetermined logic state to said processors other than said selected processor on page 4, paragraph 0058 and page 5, paragraphs 0072-0073; on page 11, paragraphs 0128,0129 and Figures 2 and 3.

8. As per claims 9 and 19, Edwards et al. discloses coupling a trace circuit to said selected processor in response to a select signal; transferring information from said selected processor to said trace circuit while said selected processor is executing said software; and presenting said information received by said trace circuit at a port; and connecting said processors and said trace circuit through a boundary scan chain on page 4, paragraph 0058 and page 5, paragraphs 0072-0073; on page 11, paragraphs 0128,0129. The trace circuit is part of the debug circuit as disclosed in Figures 2 and 3. Also see claim 1.

9. As per claim 10, Edwards et al. discloses transferring data from said trace circuit to said selected processor on page 4, paragraph 0058 and page 5, paragraphs 0072-0073.

10. As per claim 11, Edwards et al. discloses transferring a first test data stream received by said selected processor to said trace circuit on page 4, paragraph 0058 and page 5, paragraphs 0072-0073; on page 11, paragraphs 0128,0129 and Figures 2 and 3.

11. As per claim 12, Edwards et al. discloses transferring a second test data stream from said trace circuit to said selected processor on page 4, paragraph 0058 and page 5, paragraphs 0072-0073; on page 11, paragraphs 0128,0129 and Figures 2 and 3.

12. As per claim 20, Edwards et al. discloses wherein said processors, said trace circuit and said connector circuit are embedded in a single integrated circuit on page 4, paragraphs 0056-0058. Communication link 104 is the connector circuit.

Response to Arguments

13. Applicant's arguments with respect to claims 1-4,9-12,19,20 have been considered but are persuasive concerning claims 5,13,14 and not persuasive concerning the rest of the rejected claims. Applicant argues on pages 8-9 under the Remarks Section concerning claim 1, "Despite the assertion in the Office Action, the communication link 104 of Edwards...does not appear to couple in response to a select signal. Therefore, Edwards does not appear to disclose or suggest a connect circuit configured to couple a trace circuit to a selected processor of a plurality of processors in response to a select signal." Examiner respectfully disagrees.

14. Edwards select signal is the debug commands sent to the processor across the communication link to gather the information requested by the debug commands that are transferred back to the debug circuit, as disclosed on page 4, paragraph 0058.

15. Applicant also argues on page 9 under the Remarks Section concerning claim 1, "Despite the assertion in the Office Action, Edwards appears to be silent regarding a JTAG chain connected to a processor 102 (asserted similar to one of the claimed processors). Therefore, Edwards does not appear to discloses a boundary scan chain..." Examiner respectfully disagrees. Edwards discloses the 'JTAG chain' on page 5, paragraph 0076 and in Figure 3.

16. Applicant argues on pages 9-10 concerning claim 3, "Despite the assertion in the Office Action, Edwards appears to be silent regarding the communication link 104 (asserted similar to the claimed connector circuit) transferring test data streams through the JTAG chain (asserted similar to the claimed boundary scan chain)." Applicant therefore believes that the limitation of claim 3 is not disclosed in Edwards. Examiner respectfully disagrees.

17. Edwards discloses this on page 11, paragraphs 0128,0129. For the test data streams to reach the processor on the integrated circuit, the data streams have to cross the communications link.

18. Applicant argues on page 10 under the Remarks Section concerning claim 4, "Despite the assertion in the Office Action, Edwards appears to be silent regarding the communication link 104 (asserted similar to the claimed connector circuit) transferring test data streams through the JTAG chain (asserted similar to the claimed boundary scan chain)." Applicant therefore believes that Edwards fails to anticipate the limitation of claim 4. Examiner respectfully disagrees.

19. Edwards discloses this on page 11, paragraphs 0128,0129. For the test data streams to reach the processor on the integrated circuit, the data streams have to cross the communications link.

20. Applicant argues on pages 11-12 under the Remarks Section concerning claim 12, "Despite the assertion in the Office Action, Edwards appears to be silent regarding transferring test data streams from a debug circuit 103 (asserted similar to the claimed trace circuit) and the processor 102 (asserted similar to the claimed selected

processor). In particular, the only cited text of Edwards that discusses transfers from the debug circuit 103 to the processor 102 is paragraph 0058 which states that the communication link 104 transfers 'state and processor control information from the debug circuit 103 to the processor 102.' The rest of Edwards appears to be silent regards the communication link 104 transferring test data streams to the processor 102." Therefore Applicant believes that Edwards does not anticipate the limitation of claim 12. Examiner respectfully disagrees.

21. Edwards discloses this on page 4, paragraphs 0058. It is inherent in the operation of this debugging system that the test data is received as the state and control information across the link.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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